IN THE CLAIMS:

Please cancel claims 1-54 without prejudice or disclaimer.

Please add the following new claims.

55. A transportable integrated circuit chip test device comprising:

a transportable test box;

a plurality of test boards mounted in said test box; and

a portable power supply in said test box connected to said test boards,

wherein each of said test boards comprises:

sockets adapted to hold integrated circuit chips to be tested while being transported; and

testing circuitry electrically connected to said sockets.

56. The device in claim 55, wherein each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets.

57. The device in claim 55, wherein said portable power supply comprises a battery.

58. The device in claim 55, wherein each of said test boards includes a memory adapted to store test results.

59. The device in claim 55, wherein each of said test boards includes a known good integrated circuit chip.

60. The device in claim 59, wherein each of said test boards includes comparators electrically connected to said sockets.

61. The device in claim 60, wherein said testing circuitry is adapted to supply identical test patterns to said integrated circuit chips to be tested and to said known good integrated circuit chip, and

wherein said comparators compare an output generated by said known good integrated circuit chip with outputs generated by said integrated circuit chips to be tested to identify defective integrated circuit chips.

62. The device in claim 61, wherein said comparators are in parallel to one another such that all comparisons performed by said comparators are made simultaneously.

63. A transportable integrated circuit chip test device adapted to test application specific integrated circuit (ASIC) chips, said device comprising:

a transportable test box;

a plurality of test boards mounted in said test box; and

a portable power supply in said test box connected to said test boards,

wherein each of said test boards comprises:

sockets adapted to hold ASIC chips to be tested while being transported; and

testing circuitry electrically connected to said sockets, wherein said testing circuitry includes comparators arranged in parallel and electrically connected to said sockets,

such that said testing circuitry tests all of said ASIC chips simultaneously, and

wherein said testing circuitry identifies a defective ASIC chip as one having a different output when compared to outputs of the other ASIC chips, when all ASIC chips are supplied with identical inputs.

64. The device in claim, 63 wherein all of said ASIC chips have an identical design.

65. The device in claim 63, wherein each of said test boards includes visual test failure indicators, such that one of said visual test failure indicators is adjacent each of said sockets.

66. The device in claim 63, wherein said portable power supply comprises a battery.

67. The device in claim 63, wherein each of said test boards includes a memory adapted to store test results.

68. The device in claim 63, wherein each of said test boards includes a known good integrated circuit chip.

69. The device in claim 68, wherein all of said comparators are connected to said known good integrated circuit chip such that any ASIC chips that produce an output different than the output produced by said known good integrated circuit chip is identified as a defective ASIC chip.

70. The device in claim 63, wherein by comparing whether outputs of all ASIC chips are identical, said testing circuitry does not require a specific proper output that a given input should produce for the specific design of ASIC chip being tested.

71. An integrated circuit chip test device adapted to test integrated circuit chips, said device comprising:

a test board;

sockets on said test board, said sockets being adapted to hold integrated circuit chips to be tested; and

testing circuitry on said test board electrically connected to said sockets,

wherein said testing circuitry includes comparators arranged in parallel and electrically connected to said sockets, such that said testing circuitry tests all of said integrated circuit chips simultaneously, and

wherein said testing circuitry identifies a defective integrated circuit chip as one having a different output when compared to outputs of the other integrated circuit chips, when all said integrated circuit chips are supplied with identical inputs.

72. The device in claim 71, wherein all of said integrated circuit chips have an identical design.

73. The device in claim 71, further comprising visual test failure indicators attached to said test board, such that one of said visual test failure indicators is adjacent each of said sockets.

74. The device in claim 71, further comprising a memory attached to said test board, said memory being adapted to store test results.

75. The device in claim 71, further comprising a known good integrated circuit chip attached to said board.

76. The device in claim 75, wherein all of said comparators are connected to said known good integrated circuit chip such that any integrated circuit chips that produce an output different than the output produced by said known good integrated circuit chip is identified as a defective integrated circuit chip.

77. The device in claim 71, wherein by comparing whether outputs of all integrated circuit chips are identical, said testing circuitry does not require a specific proper output that a given input should produce for the specific design of the integrated circuit chip being tested.

78. An integrated circuit chip test device adapted to test integrated circuit chips, said device comprising:

a test board;

sockets on said test board, said sockets being adapted to hold integrated circuit chips to be tested;

testing circuitry on said test board electrically connected to said sockets; and

a golden socket for a known good integrated circuit chip,

wherein said testing circuitry includes comparators arranged in parallel and electrically connected to said sockets, such that said testing circuitry tests all of said integrated circuit chips simultaneously, and

wherein said testing circuitry identifies a defective integrated circuit chip as one having a

different output when compared to outputs of the other integrated circuit chips and the output of said known good integrated circuit chip, when all said integrated circuit chips and said known good integrated circuit chip are supplied with identical inputs.

79. The device in claim 78, wherein all of said integrated circuit chips have an identical design.

80. The device in claim 78, further comprising visual test failure indicators attached to said test board, such that one of said visual test failure indicators is adjacent each of said sockets.

81. The device in claim 78, further comprising a memory attached to said test board, said memory being adapted to store test results.

82. The device in claim 78, wherein all of said comparators are connected to said known good integrated circuit chip such that any integrated circuit chips that produce an output different than the output produced by said known good integrated circuit chip is identified as a defective integrated circuit chip.

83. The device in claim 78, wherein by comparing whether outputs of all integrated circuit chips are identical, said testing circuitry does not require a specific proper output that a given input should produce for the specific design of the integrated circuit chip being tested.